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Methods and Designs for Improving Operational Amplifier Performance

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Abstract:

This paper reviews recent improvements in operational amplifier design, focusing on key performance aspects such as noise reduction, gain enhancement, gain-bandwidth product improvement, accuracy enhancement, slew rate improvement, and bandwidth increase. The article begins by explaining the fundamental principles of operational amplifiers, including open-loop gain, bandwidth, and noise sources. It then explores various design modifications aimed at enhancing specific characteristics. Five innovative designs are presented: a CMOS operational amplifier with high gain and output swing, a two-stage amplifier with improved unity gain bandwidth, a highly linear and high-gain operational amplifier using cross-coupled differential pairs and positive feedback, a high-gain rail-to-rail operational amplifier with folded cascade structure, and an operational transconductance amplifier with enhanced gain-bandwidth product and slew rate. Each design is described in terms of its unique features, circuit structure, and performance improvements. The paper highlights the continuous evolution of operational amplifier technology to meet the increasing demands of modern electronic applications across various fields.

Keywords: Amplifier; gain-bandwidth; noise reduction.

1. Introduction

An operational amplifier, or op-amp for short, is a basic electronic component. The fundamental function of an op-amp is to magnify the input voltage, and the magnification of it is so large that it can be ten thousand or higher. The types of operational amplifiers include dual power operational amplifiers, single power operational amplifiers, and rail to rail operational amplifiers. In addition, operational amplifiers can be classified according to different characteristics, such as general-purpose, high impedance, low-temperature drift, high-speed, low-power, and high-voltage high-power. So far, a variety of uses of the operational amplifier on circuits have been developed. When it is working in the linear region, integrated operational amplifiers can achieve various operational functions such as in-phase ratio, inverse ratio, addition, subtraction, differentiation, integration, etc.. At the same time, integrated operational amplifiers can also achieve waveform transformation, waveform generation, rectification, filtering, and mutual transformation of voltage and current in its linear region

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[1]. Moreover, the nonlinear applications of integrated operational amplifiers include generating square waves, rectangular waves, triangular waves, and sawtooth waves; waveform transformation, shaping, and level detection; Integrated circuits [1]. In macro, operational amplifiers are widely used in public, household, commercial, and industrial fields, including alarms, light sensors, radios, and links. An op-amp can also send a series of signals, which can be used to control applications to control machinery. So, operational amplifier is very important to human life and industry. However, with the development of the electronic technology and the increased demand, the requirements and the standard of an operational amplifier are elevated. Then, many newly designs of operational amplifier, the modification methods, are proposed. This paper will focus on making a review of the recent improved designs of operational amplifier about reducing noise, increasing gain, proving gain bandwidth product, improving accuracy, enhancing slew rate, and increasing bandwidth.

2. Operational amplifier

Open loop gain is the amplification factor of the input signal or voltage of an operational amplifier without feedback. The equation is:

$$G = \frac{Vout}{Vin} \tag{1}$$

The operational amplifier's bandwidth serves as an indicator of its capacity to handle signals across various frequencies. A wider bandwidth allows for processing higher frequency signals, resulting in superior high-frequency performance. However, when the amplified signal's frequency surpasses the bandwidth, distortion occurs and intensifies as frequency increases.

An amplifier's gain bandwidth product is obtained by multiplying its frequency by the corresponding gain. This product remains constant within the operational amplifier's linear operating range. As frequency rises, gain diminishes. The open-loop gain curve of an operational amplifier provides a clear visual representation of the gain bandwidth product.

Seymour Letzter and Norman Webster define noise as "voltages and currents that accompany and obscure a desired signal. Numerous noise types originate from various sources, including electrical components like amplifiers and signal processing instruments. Non-electrical sources can also generate electrical fluctuations when system elements act as transducers. For instance, structural vibrations transmitted to coaxial cables may induce signals due to dimensional changes, resulting in capacitive variations in the cable" [2]. Additionally, electrical circuits commonly experience five noise types: shot noise, Johnson (thermal) noise, flicker noise, burst noise, and avalanche noise [3].

The maximum rate at which an op-amp's output circuitry can change voltage is known as the slew rate. Typically measured in volts per microsecond (V/µs) in datasheets, it is time-related. Slewing is a non-linear phenomenon. When the product of the op-amp's gain and the slope of a sinusoidal input signal exceeds its slew rate, the output waveform exhibits a straight segment instead of a curved one. Consequently, slewing can introduce distortion and alter a signal's amplitude or phase. The operational amplifier's slew rate is:

$$SR = \frac{dV}{dt} \tag{2}$$

Where SR represents the slew rate, V represents the voltage, t represents the time.

3. Improving the specific aspect of the operational amplifier

3.1 A CMOS operational amplifier design

This paper examines a two-stage CMOS operational amplifier design, featuring a differential amplifier in the initial stage, coupled with a compensating capacitor and a high-gain stage. The OpAmp was designed and simulated using the Cadence Virtuoso 180 nm CMOS process, operating on a single 0-3.3 V power supply.

The circuit employs PMOS transistors M3 and M4 in current mirror configuration, ensuring identical aspect ratios. To optimize output stage gain, PMOS transistor M6 and NMOS transistor M7 are utilized. The design replaces the conventional current biasing Idc with an active load resistor (PMOS transistors: M9, M10, M11), facilitating layout design and reducing both area and power consumption compared to traditional two-stage Op-Amp designs.

As illustrated in Fig. 1, the Compensation Capacitor (CC) is set to 800fF, while the Load Capacitor (CL) is 2pF. This configuration achieves high gain and output swing while minimizing power dissipation, demonstrating improved performance over conventional OpAmp designs.

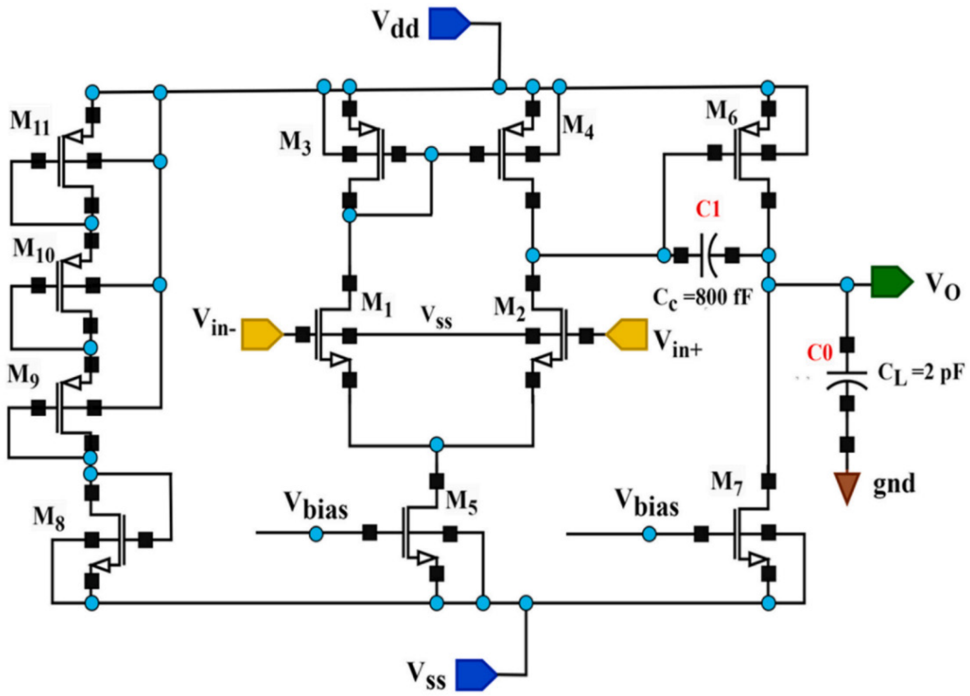

Fig. 1 A CMOS operational amplifier design [4].

This design approach simplifies layout creation while minimizing both area and power consumption compared to conventional two-stage operational amplifier designs. The proposed OpAmp achieves impressive performance metrics, including a 62.9449 dB gain, 92.80792 dB CMRR, 33 MHz unity gain bandwidth, and an optimized layout area of 0.001476 µm2. These results indicate that the amplifier meets or exceeds all predetermined design specifications. Future research avenues, such as enhancing robustness, reliability, and integration with cutting-edge sensor technologies, are outlined to address evolving industrial and biomedical application requirements.

3.2 A Design and Analysis of a Two Stage Operational Amplifier for High Gain and High Bandwidth

This research explores an operational amplifier design utilizing RC Miller compensation, implemented in a 0.18 µm CMOS process with TSMC libraries. The architecture incorporates a differential pair amplifier (A1) and a common source amplifier (A2). Biasing is provided by a single 50 µA reference current source, eliminating the need for separate voltage sources. The compensation circuit employs RC Miller frequency compensation, featuring a series-connected resistor and a 0.9 pF compensation capacitor (Cc) [5].

By increasing the bias current, the study achieves a remarkable 136.8 MHz unity gain bandwidth while maintaining a high gain of 92.27 dB. This approach offers an effective method for controlling bandwidth expansion. The design addresses the challenge of fabricating large resistors in modern VLSI technology by implementing the series compensation resistor as a PMOS transistor operating in the triode region.

The elimination of external voltage sources for biasing results in reduced packaging costs by removing additional DC bias voltage source pins. However, it's worth noting that the increased bias current leads to a trade-off, resulting in lower DC gain and higher power dissipation. This design presents an innovative solution for high-performance operational amplifiers, balancing bandwidth, gain, and power considerations in modern CMOS processes.

3.3 A highly linear and high gain operational amplifier

This paper introduces an innovative Op-Amp design, characterized by high gain and exceptional linearity. The circuit's architecture, depicted in Fig. 2, incorporates a cross-coupled differential pair and positive feedback. The Op-Amp's differential amplifier comprises two stages: the first producing a differential output, while the second amplifies the circuit's difference as its output. An additional stage, utilizing a simple current sink inverter, completes the amplifier's structure.

The proposed design features matched transistor pairs: M1 & M2, M3 & M4, M7 & M8 (both a & b), and M11 & M12. The cross-coupled differential pair consists of M1, M2, M3, and M4. Active loads, formed by M7a,

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M7b, M8a, and M8b, convert the current output from the differential pair into voltage. Positive feedback is implemented through M9 and M10, which are also cross-coupled. These transistors sense output voltages and regulate current flow into the differential stage, functioning as a feedback mechanism that enhances amplification.

Current mirroring occurs through M11 and M12, where the amplified differential voltage is obtained. The final stage, composed of M14 and M15, further amplifies the signal and ensures circuit stability.

Designed using the UMC90nm library in Cadence virtuoso analog design environment for a 0.18μm CMOS process, the Op-Amp demonstrates impressive performance. Simulations reveal a gain of 124dB, a unity gain bandwidth of 307MHz, and a phase margin of 69 degrees, while consuming 221μW of power. THD analysis indicates a maximum distortion of 63dB at 2V output peak-to-peak voltage and 1KHz frequency [6].

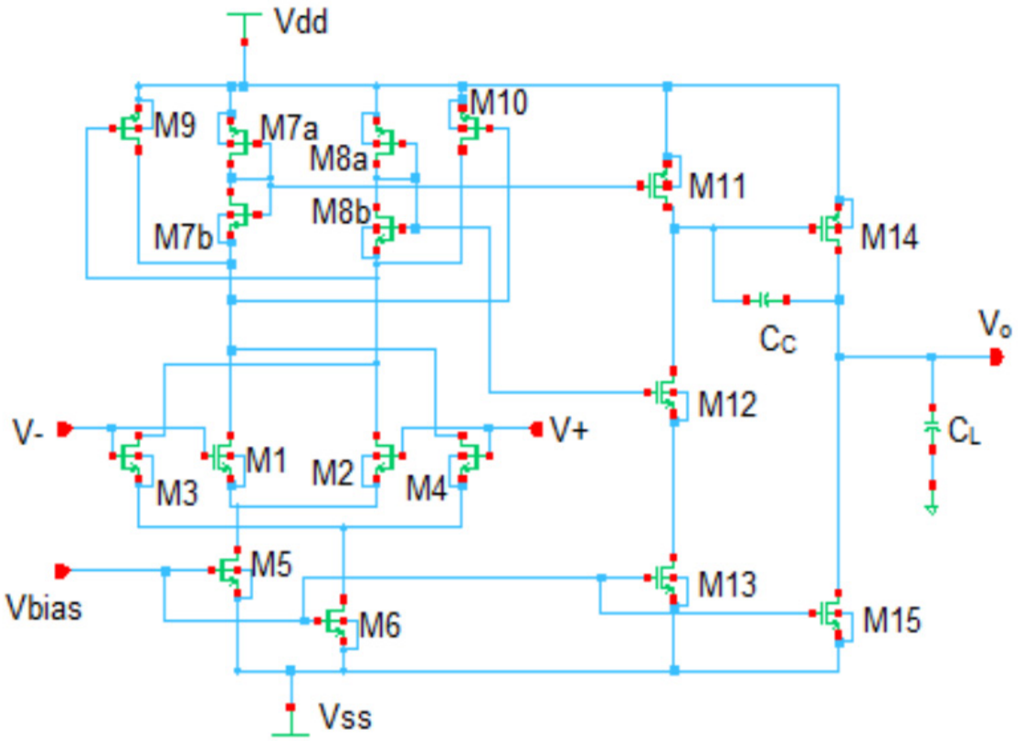

Fig. 2 A highly linear and high gain operational amplifier [6].

3.4 Design and Analysis of a High-Gain Rail-To-Rail Operational Amplifier

This study presents an operational amplifier design utilizing the TSMC 0.35um CMOS process, incorporating a folded cascode structure and a class AB output stage. The main op-amp circuit, illustrated in Fig. 3, employs a folded cascode configuration. Transistors M3, M4, and M5 provide current bias, ensuring optimal gain and slew rate performance.

The folded structure is formed by M1, M2, M6, and M7, while M8, M9, and M10 constitute a cascode current mirror load. This arrangement facilitates the conversion of differential input to single-ended output. The chosen circuit topology effectively enhances output impedance while maintaining circuit speed, making it a popular choice in op-amp design.

Although the folded cascode structure improves output resistance, it also impacts voltage swing due to transistor saturation voltage drop. To address this, the proposed amplifier implements a class AB output structure. To ensure stable operation and prevent oscillation, Miller compensation principles are applied, introducing compensation capacitors C1 and C2.

Circuit simulation was conducted using Hspice 2004 software. The results demonstrate impressive performance characteristics, including high gain and low static power consumption. Specifically, the design achieves an open-loop gain exceeding 96dB, a bandwidth of 127MHz, and a phase margin of 63.4 degrees. Additionally, the circuit exhibits a CMRR of 131.5dB and a power supply rejection ratio of 78dB [7].

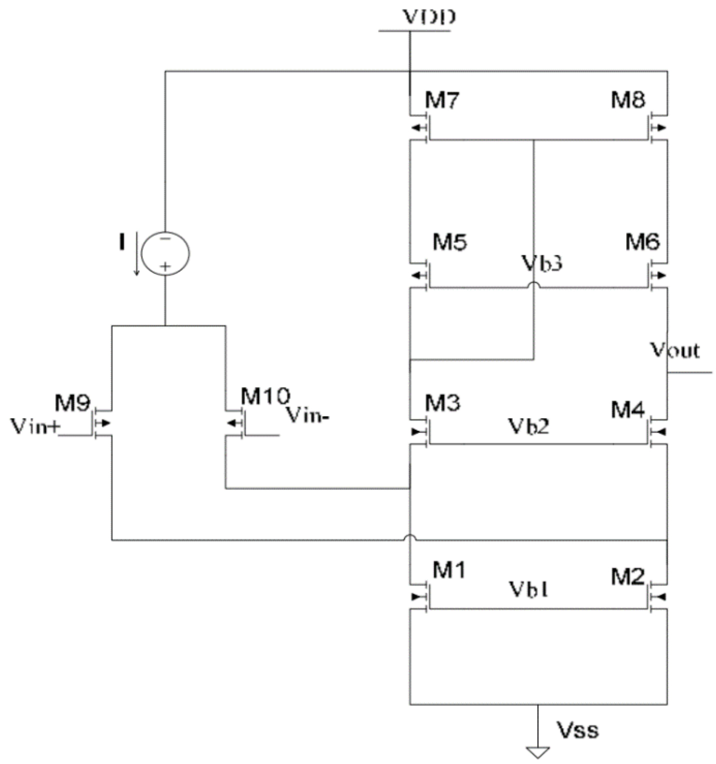

Fig. 3 High-Gain Rail-To-Rail Operational Amplifier [7].

3.5 An operational transconductance amplifier with high gain-bandwidth product and high swing rate

It consists of an adaptive bias circuit, a feedback loop, and a folded cascode operational amplifier. Among them, the adaptive bias circuit uses a flip voltage follower (FVF) to achieve. The transistors M11, M13, and M15 form an FVF, and the transistors M12, M14, and M16 form another FVF. The two FVFs are cross-coupled to the differential input pair; the feedback loop is composed of input transistor M1 (M2), folded current source tube M3 (M4), adaptive bias circuit, current mirror transistor M17 (M18), M21 (M22) and transistor M19 (M20) as resistance. Transistors M5 (M6), M7 (M8) and M9 (M10) constitute the output stage of the operational amplifier.

The improved folded cascode operational transconductance amplifier provides a variable bias current to the circuit through an adaptive bias circuit, thereby increasing the dynamic current and gain bandwidth product ; using the feedback circuit to fold the current source; the transistor is fully utilized, so that it cannot only generate current, but also provide a certain transconductance for the operational amplifier ; it is allowed to pass a large dynamic current without being limited by a static current, so that the slew rate is improved. The simulation results show that the gain bandwidth product is about 9 times and 4 times higher than that of the traditional folded cascode operational amplifier and the multiplexed folded cascode operational amplifier, respectively [8].

4 Conclusion

In conclusion, this review of recent operational amplifier designs demonstrates significant advancements in key performance metrics. The CMOS operational amplifier achieved high gain and output swing with reduced power dissipation, while the two-stage amplifier improved unity gain bandwidth through increased bias current. The highly linear and high-gain design utilized cross-coupled differential pairs and positive feedback to achieve impressive gain and linearity. The high-gain rail-to-rail amplifier employed a folded cascode structure to enhance output resistance and voltage swing. Lastly, the operational transconductance amplifier with adaptive biasing showed remarkable improvements in gain-bandwidth product and slew rate.

These innovations address critical challenges in operational amplifier design, such as balancing high gain with wide bandwidth, maintaining linearity, and optimizing power consumption. The diverse approaches presented highlight the multifaceted nature of amplifier design, where trade-offs between various performance parameters must be carefully managed.

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As electronic systems continue to evolve, demanding higher speed, precision, and efficiency, further research in operational amplifier design remains crucial. Future directions may include exploring novel materials, advanced fabrication techniques, and innovative circuit topologies to push the boundaries of amplifier performance. Additionally, addressing emerging applications in fields such as IoT, 5G communications, and biomedical devices will likely drive new design priorities and challenges in operational amplifier technology.

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