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A Research of the Integrated Circuit Design and Optimization

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Abstract:

With the scientific and technical revolution going on, integrated circuit has been playing a vital role in our daily life ever since. In IC (Integrated circuit) design and manufacturing, layout of the integrated circuit determines its success or failure. However, the constantly decreasing characteristic size and progressive process bring about some new issues. That is why in post-Moore's Law period, the design and optimization of layouts deserves attention of the whole industry. A properly designed and optimized layout not only results in better performance while using, but also cut out the cost of manufacture. In this paper, the methodology of integrated circuit layout design and optimization are discussed. For design, the author presented the whole flow of how the layout is generated and principles in integrated circuit design. For optimization, two approaches are analyzed. One is shorting out the critical area. Based on critical area theory and methodology of image processing, layouts can be improved in configuration. The method discussed here makes a modification on the previous way to make the optimization more accurate and efficient. The other method is inserting auxiliary polysilicon, which can counteract the impact of channel length change of MOSFETs and focus error as a unavoidable result of the process improvement.

Keywords: Integrated Circuit; Circuit Design; Layout optimization; Critical Area; Polysilicon width

1. Introduction

Integrated circuit is the brain of the modern industry. As the bond of the national science and technology strategy and industry development, the level of the integrated circuit industry reflects the level of innovation and manufacture of a country to some extent [1]. From the birth of the first computer in 1832 to Zuse Z3, ENIAC to the first PC Simon, from the transistor revolution in 1948 to the birth of integrated circuit in 1958, the development of integrated circuit has been following the Moore's Law over the few decades — the number of transistors in a dense integrated circuit doubles about every 18 months, while the cost of the computing halves. With the rapid development of the integrated circuit industry, which went through small scale, medium scale, large scale, VLSI (Very Large Scale Integration) and ULSI (Ultra Large Scale Integration) [2], various kinds of chips are used more widely than ever in our daily lives. As the bridge connecting the integrated circuit design and manufacturing, the imaging quality from layout to silicon wafer directly determines the success a chip [3]. To meet the expected requirements, some failure caused by place and routing or the self-performance of the device may appear unavoidably during the designing process. A high-quality layout can remarkably decrease the cost of the production of the chips and guarantee the yield and actual performance, in this case, the proper design and optimization of the layout remain to be the focus for the integrated circuit industry to develop and most of the research.

The article starts with the integrated circuit design, expounding the overall procedure the designing from logic design to the final GDSII based on the common theories of the industry. This part shows how to connect the integrated circuit design and fabrication with layout. After that, some principles and warnings are given to remind the designers to achieve the high-quality design to maximum. For the layout optimization, the article introduces two theories — shorting out the critical area and inserting the auxiliary polysilicon — to demonstrate the vital impact of the layout optimization. With a simple introduction and comparison, it is indicated that these two methods can bring improvements to the performance of the circuit on different levels.

The article is arranged as follows. Section 1 is introduction of the whole passage, introducing the background of the integrated circuit industry and the significance of the research. Section 2 describes the flow of design, the basic principles and some important matters to notice. Section 3 presents two approaches to optimize the layout of an integrated circuit and makes a comparison between them. Section 4 summarizes the conclusions drawn in this article

and points out the future directions of the research.

2. Integrated Circuit Design

2.1 The Flow of Layout Design

The overall process of the integrated circuit design can be divided into several following steps. The first of all is logic design. With Verilog, designers can make a conversion from expected function to logic language. The second step is logic synthesis. In this step, logic languages are turned into gate level netlist. The third step is to get the floorplan with EDA tools. In the fourth step, designers need to place and route the actual tools in the circuit with the layout of arrangement acquired in the last step. It should be noted that after the third and fourth step, timing check is needed to ensure the circuit can meet the required function. If failures appear, designers need to go back to logic design and the following steps until the circuit pass the timing check. Then GDSII is generated. By adding digital libraries to GDSII, designers can get a layout file including the devices. The final step is DRC and LVS check. With both DRC and LVS checks passed, the GDSII file which can satisfy the intended needs is finally acquired. The flow chart is shown in figure 1.

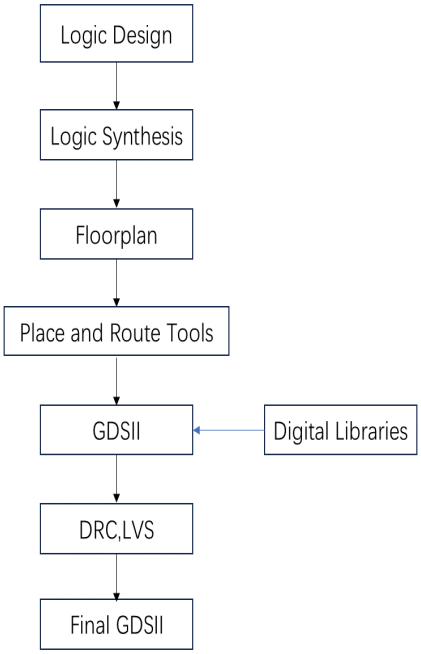

Fig. 1 The flow chart of layout design of an integrated circuit

2.2 The Principle of Layout Design

Classified by the degree of automation, the layout design of an integrated circuit can be divided into manual design and automation design; while classified by limits of layout module, the layout design of an integrated circuit can be divided into semi-custom and fully custom. The layout of an integrated circuit pursues compaction and high efficiency, which means designers need to use the area and devices as little as possible to achieve the desired function and maximized yield. To be more specific, there are three main goals to achieve: the first one is to reduce the wiring in the circuit, including both the amount and complexity. Less wiring leads to shorter dely. The second goal is to increase the integration of the chip. A well -designed layout takes up the minimum area and cut the cost of manufacture. The third goal is also the most basic one, is to meet the acceptance standard, which needs an integrated circuit to meet the requirements and improve the performance.

Layout design includes several aspects. Transistors, elementary unit module and complex unit module need to be well placed. In addition, designers should organize the position and size of each unit on every process layer according to the layout. After overall planning, designers need to optimize the routing between each unit.

2.2 Matters Need Attention in Layout Design

There are different designing rules for different process according to different manufacturers. Even the digital circuit and analog circuit design are different form each other. In digital circuit, layout of different quality affects the transmission speed of a circuit. In digital design, designers need to lower the transmission delay of a signal or match the devices, while reduce the area of the chip to cut down the cost. In analog design, layouts not only affect the speed performance, but also determines the accuracy of the circuits. Hence, when designing analog circuit, the symmetry of the layout, matching between devices, parasitism and imbalance and interference between signals are all need to be taken into consideration.

When designing circuits, designers should also pay attention to some mechanism which could lead to circuit failure such as antenna effect, soft connection, latch-up, electro-migration, metal stress and density. Avoiding these loopholes caused by inconsiderable design can vastly simplify the optimization afterwards and improve the efficiency and quality.

3. Layout Optimization

3.1 Shorting Out Critical Area to Optimize Layout

With the characteristic dimension of devices reducing from micron level to sub-micron, deep sub-micron, integration level constantly improved [4]. Defects caused by process is unavoidable, which is one of the main reasons for yield reduction. Circuits inevitably fail when defects

happen in some certain areas [5]. Critical area is the measure of these important areas, reflecting the sensitivity of the chips to defects and deviation [6,7].

To reduce the impact of defects on integrated circuits, except from improving the process, optimizing the layout is also a crucial approach. The methodology discussed here uses math morphology as assistance to deal with the image of layouts and reduce the critical area by expansion and erosion algorithm in order to optimize the layouts [8].

As a common way of optimization, traditional practice compares the critical area reduced to determine which is the best spot for netlists to move. The operation discussed in this article made an improvement to detect the available space for the netlist to move in the first place. Using the critical area caused by defects to determine how should the netlist move, scilicet movable space algorithm, especially when optimizing tiny critical area, designers can move the netlist partly, which can enormously improve the optimization efficiency.

The optimization steps are as follows. After visualization of the layout, designers need to make statistics of each netlist's space for optimization. The detailed method is to use the structural element which is the same size of the defect size to expand the framework of the netlist until netlists intersect their surroundings. The difference between the original and expanded size of the structural element are is the available space for optimization. By comparing the reduction value of each netlist under the circumstance of certain defect, designers should optimize each netlist from great to small [9].

3.2 Inserting Auxiliary Polysilicon to Optimize Layout

In post-Moore's law period, the space between devices decreased along with continuous reduction of the characteristic size, resulting in the greater influence of certain parasitic parameters on a chip [10]. The configuration of devices affects the manufacturing process results, thus changing the channel stress and causing the circuit performance to change [11]. A main reason for low yield is the change of polysilicon width, also known as the channel length of MOSFET. Situations such as suboptimal exposure system in lithography, mask failure, uneven photoresist, exposure dose change, focus error, micro loading effect and unqualified lens may give rise to channel length change [12]. Polysilicon width varies with the space between its adjacent polysilicon. The smaller the width, the more likely the performance parameters such as sub threshold current may change. The method discussed below aims at diminishing the impact of focus error and the space between polysilicon on channel length by inserting auxiliary polysilicon as the figure 2 shows [13].

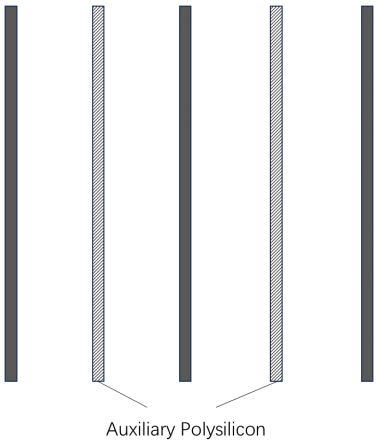

Fig. 2 After inserting the polysilicon

The core of the method is to fill the space between two adjacent units with polysilicon. The following is the detailed practice. First, designers should extract the characteristic graphic of the polysilicon of each MOSFET on the edge of the standard unit. By adjusting the number and width of each polysilicon and space between each other and photoetching simulation, the best auxiliary polysilicon for different shapes of polysilicon and a table of channel length change can be acquired. For different layouts, designers can lookup the table and determine which is the best auxiliary polysilicon to use. Auxiliary polysilicon can reduce the influence of polysilicon width and focus error at the same time.

3.3 Comparison Between Two Methods

Both of the two methods discussed in the article have their advantages. Shorting out the critical area aims at resolving the problems caused by defects at the level of the whole layout. With an overall comparison of all the movable space in the previous stage, designers can settle the sequence of optimization for each netlist more accurately and scientifically. Based on the analysis of critical area, this approach makes an improvement on the previous methodology at assuming the movable position, making it more efficient and accurate.

The method of inserting auxiliary polysilicon put forward a way to optimize layouts at the device level. By fixing the failure caused by channel length change of MOSFETs and focus error, the method decreases the performance deviation of devices, which is more rooted and thorough.

4. Summary

As the challenge the industry is actually facing, the article analyses the integrated circuit design and layout optimization by demonstrating the designing process in detail and comparing different optimization methods. During design-

ing, while trying to satisfy expected requirements, designers need to put the basic principles in the first place and pay attention to some specific design which could cause the circuit to fail. Layout optimization is the key step in integrated circuit fabrication. The methods of shorting out the critical area and inserting auxiliary polysilicon to optimize the layout are discussed and compared. The former adjust the overall arrangement of the devices and wiring to make optimization. While the critical area cause by defect can be acquired and decreased by expansion algorithm and corrosion principle in math morphology, the method mentioned in the article adds the step of space detection and overall planning to improve the efficiency. The second approach aims to fix the circuit failure caused by devices and integrated circuit process. Auxiliary polysilicon can make up the polysilicon width, namely the channel length of MOSFET.

Due to limited academic competence and experience, there are some aspects to be perfected in this article. Integrated circuit design varies from situation to situation. Therefore, it cannot be generalized briefly. Only the common methodologies and principles are discussed here. In circuit optimization, there are masses of optimization means. The two approaches presented in the article may not be appropriated for every circuit. Designers need to take actual need and real situation into consideration to decide which method to choose. Moreover, neither of the methods discussed the power dissipation and time delay, which is key factor in assessing the practicability of an integrated circuit. In conclusion, there are far more aspects and different dimensions to optimize the layout. With more refined design and more practicable optimization found, the manufacture of integrated circuit will move toward a more efficient, energy-saving, and cheap direction.

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