ISSN 2959-6157

Research of Gate-All-Around Field-Effect Transistors

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Abstract:

This report provides an overview of GAA FETs also known as Gate-All-Around FETs, focusing on their introduction and limitations, based on a comprehensive review of current literature and online resources. GAA FETs represent an evolution of FinFET technology, which itself was developed from traditional MOSFET designs. Each iteration has aimed to improve performance and overcome limitations of its predecessor. The GAA architecture offers superior electrostatic control, resulting in higher drive currents, reduced leakage, and improved subthreshold swing, making it ideal for high-performance, low-power applications. Despite these advantages, GAA FETs still face challenges with short-channel effects (SCEs) as device dimensions shrink. Gate-All-Around (GAA) is a transistor architecture designed to address the limitations of the FinFET design. Unlike FinFET, where the channel is surrounded on three sides by the gate, GAA surrounds the channel on all four sides by turning the FinFET structure sideways, making the channels horizontal. This design provides enhanced control over the transistor switch. The fabrication of GAA transistors involves a series of highly precise processes, which enable improved transistor scaling with reduced variability, resulting in increased performance and lower power consumption.

Keywords: Transistor, Field effect transistor, Gate all around

1. Introduction

Over the past decade, GAA FETs, have emerged as a major advancement in semiconductor technology. These devices play a crucial role in the ongoing effort to sustain Moore's Law, which predicts the doubling of transistor density on integrated circuits approximately every two years. As traditional FinFETs (Fin Field-Effect Transistors) approach their scaling limits, GAA FETs provide a new architecture that allows for further miniaturization of transistors while maintaining performance. In GAA FETs, the gate surrounds the channel on all sides, offering better electrostatic control compared to previous designs like FinFETs, where the gate only wraps around three sides. This all-around control reduces current leakage, leading to lower power consumption and improved efficiency, which is crucial for battery-powered devices like smartphones and laptops. The growth in the semiconductor market has led to improved transistor performance, but it has also exacerbated the issue of Short-Channel Effects (SCEs) [1]. To address the SCE problem, significant changes in transistor design have been introduced. Many researchers now believe that the vertically stacked nanowire (VS-NW) structure could be a promising solution to these challenges, as it offers improved electrostatic control and scalability compared to planar structures.

This report will delve into the development and advantages of three distinct GAA FET designs—Ribbon, Vertical Transport (VT), and Forksheet FETs. Each of these architectures presents unique solutions to the challenges of modern electronics, such as improving performance scaling, enhancing power efficiency, and facilitating device integration. Ribbon FETs offer a broad channel for high drive current, VT FETs leverage vertical design for compact integration, and Forksheet FETs enable tighter gate pitch for better scaling. Together, these innovations are paving the way for the next generation of semiconductor devices, ensuring that Moore's Law continues to drive technological progress in an increasingly connected and data-driven world.

GAA FETs represent a key advancement in semiconductor technology, offering superior electrostatic control by fully surrounding the channel with the gate. This design addresses the limitations of FinFETs, particularly in reducing leakage and enhancing scalability at nodes below 5nm. Variants like nanosheet and nanowire FETs further optimize performance and efficiency [2]. While GAA FETs bring new manufacturing and material challenges, they are poised to replace FinFETs as the foundation for future semiconductor technologies. This essay will examine their development, advantages, and challenges, underscoring their importance in next-generation electronics.

2. GAA FET

As the industry pushes towards smaller technology nodes, such as 3nm and beyond, the channel length continues to decrease. At these dimensions, even with the enhanced gate control of GAA FETs, the distance between the source and drain is so short that SCEs can still occur, leading to issues like drain-induced barrier lowering (DIBL) and threshold voltage roll-off. Furthermore, The choice of channel material and the precise geometry of the transistor can significantly influence the effectiveness of channel control in GAA FETs, despite their superior performance compared to previous architectures. Variations in these factors can lead to non-uniform electric fields, which can exacerbate SCEs.

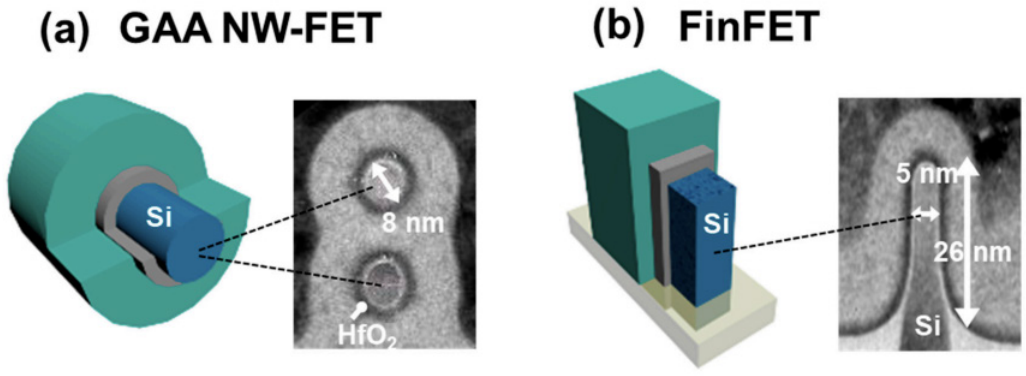

Fig. 1 TEM cross-sectional images of NMOS: (a) gate-all-around nanowire field effect transistors (GAA NW-FETs); and (b) fin field effect transistors (FinFETs). Two nanowires are stacked in GAA NW-FETs [3].

The Figure.1 compares two advanced transistor architectures: the Gate-All-Around Nanowire Field-Effect Transistor (GAA NW-FET) and the Fin Field-Effect Transistor (FinFET). In the GAA NW-FET (a), a silicon (Si) nanowire is fully surrounded by a gate material, typically a high-k dielectric like hafnium dioxide (HfO_2). The cross-sectional view shows that the nanowire has a diameter of 8 nm, offering superior electrostatic control due to the gate's complete enclosure of the channel. This structure minimizes leakage and enhances performance, making it highly scalable for future technology nodes.

In contrast, the FinFET (b) features a vertical Si fin that protrudes from the substrate, with the gate wrapping around three sides of the fin. The cross-sectional view indicates a fin width of 5 nm and a height of 26 nm. While FinFETs offer better control than traditional planar transistors by increasing the gate-channel contact area, they provide less control than GAA NW-FETs.Overall, the figure highlights the evolution from FinFETs to GAA NW-FETs as semiconductor technology advances, emphasizing the enhanced gate control and potential for scaling provided by the GAA NW-FET structure.

2.1 Ribbon FET

Ribbon FETs are an evolution of the Gate-All-Around (GAA) FET design, where the channel consists of multiple stacked nanosheets or "ribbons" surrounded by the gate on all sides. This structure allows for enhanced control over the channel, reducing short-channel effects and improving both power efficiency and drive current. Ribbon FETs are particularly suited for advanced semiconductor nodes where traditional FinFETs are less effective. Graphene nano-ribbon (GNR) field-effect transistor (FET)is a example of Ribbon FET, The resistivity of GNRs increases as the width decreases, which is attributed to the impact of edge states and boundary roughness. This suggests that as the ribbons become narrower, the influence of the edges becomes more significant, affecting the electrical properties [4].

2.2 Vt FET

Vertical Transport FETs (VT FETs) feature a unique structure where the current flows vertically through the channel, distinguishing them from traditional planar designs as shown in Figure 2. This design allows for a smaller footprint on the chip, enabling higher transistor density, which is crucial for scaling down to smaller nodes. Vt FETs can achieve high drive currents and lower leakage, making them ideal for applications requiring high performance and low power consumption. The vertical tunnel FET exhibits extremely low source-drain off-currents, high speed, and temperature-independent behavior. These characteristics make it a promising candidate for future low-power and analog applications [5].

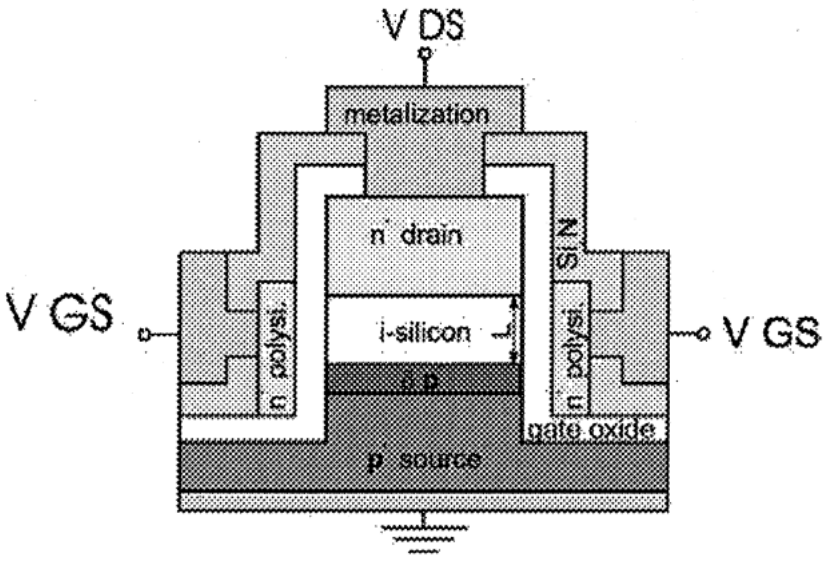

Fig. 2 Schematic representation of a vertical tunnel FET. The channel length

L = 100 nm [5].

2.3 Forksheet FET

Forksheet FETs represent a cutting-edge innovation in transistor technology, ingeniously combining the strengths of both GAA and FinFET designs to overcome scaling limitations. In Figure 3(a) FinFET and (b) Nanosheet (NSH) transistors, (c) the forksheet (FSH) architecture is being considered for future logic technology nodes. Nonetheless, the lack of fully surrounding gates and the presence of a SiN-based dielectric wall raise concerns about its reliability. In a Forksheet FET, the channels are placed side by side with a narrow "forked" gate structure between them, allowing for tighter packing of transistors without increasing the overall footprint. This design helps improve performance by enabling better electrostatic control and reducing parasitic capacitance, making Forksheet FETs a promising solution for future technology nodes. The Forksheet design, with its vertically stacked n- and p-type sheets separated by a dielectric wall, allows for more efficient scaling of logic cell track height. This is particularly advantageous as it enables further miniaturization of semiconductor devices without compromising performance [6].

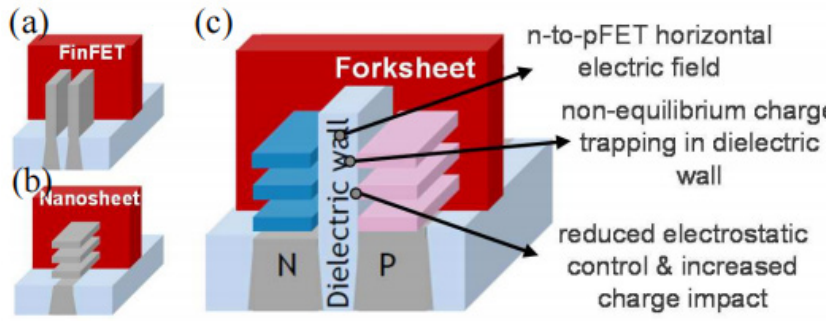

Fig. 3 FinFET and (b) Nanosheet (NSH) transistors [6]

3. Performance Evaluation of GAA FETs

The Gate-All-Around (GAA) FETs have shown remarkable promise as a successor to the FinFETs, particularly as semiconductor technology approaches the sub-5nm node. The performance of GAA FETs has been rigorously evaluated through various metrics, including drive current, leakage current, subthreshold swing, and short-channel effects (SCEs). Studies have shown significant improvements in these areas compared to traditional FinFETs, with some reports indicating up to 30% increase in drive current and 50% reduction in leakage current.

3.1 Drive Current and Transconductance

One of the most significant advantages observed in GAA FETs is their high drive current, which can be attributed to the enhanced electrostatic control provided by the gate surrounding the channel. The experimental data indicate that GAA FETs exhibit a higher on-current compared to traditional FinFETs, especially at smaller node scales. This is primarily due to the gate's ability to effectively control the entire channel, reducing the effects of quantum capacitance and improving carrier mobility. Furthermore, the transconductance (gm) of GAA FETs is also superior, indicating better amplification characteristics and higher switching speeds. This makes GAA FETs particularly suitable for high-speed and low-power applications, where performance and efficiency are paramount.

3.2 Leakage Current and Subthreshold Swing

Compared to FinFETs, GAA FETs exhibit significantly reduced leakage currents in the off-state, a crucial advancement for improving overall device efficiency. The results show that the all-around gate structure minimizes the leakage pathways, thereby reducing the off-state power dissipation. This characteristic is crucial for portable and battery-operated devices where power efficiency is a critical design parameter. The subthreshold swing (SS) in GAA FETs has also been observed to be lower than in FinFETs. This lower SS indicates a sharper turn-on characteristic, which is essential for reducing power consumption and improving switching performance. However, it's important to note that at extremely scaled-down nodes, maintaining a low SS while managing SCEs remains a challenge.

3.3 Short-Channel Effects (SCEs) in GAA FETs

Despite the improvements in gate control, GAA FETs are not entirely immune to SCEs, particularly as device dimensions continue to shrink. The experimental results reveal that at technology nodes of 3nm and below, SCEs such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off are still present, albeit to a lesser extent than in Fin FETs.

3.4 Drain-Induced Barrier Lowering (DIBL)

DIBL, a critical short-channel effect, continues to pose challenges for GAA FETs, particularly as device dimensions shrink to ultra-scaled nodes. This effect can compromise the transistor's ability to maintain a stable threshold voltage, potentially impacting overall device performance and reliability. The study found that although GAA FETs exhibit reduced DIBL compared to FinFETs, the effect becomes more pronounced as the gate length decreases. This suggests that while GAA architecture provides better control over the channel, further innovations in material engineering and device structure are necessary to mitigate DIBL effectively at sub-3nm nodes.

3.5 Threshold Voltage Roll-Off

Threshold voltage roll-off, another significant SCE in GAA FETs, manifests as a decrease in threshold voltage as the channel length shortens. This phenomenon can lead to substantial variability in device performance, particularly in ultra-scaled nodes where precise control of threshold voltage is crucial for maintaining consistent operation. This roll-off is less severe than in FinFETs due to the superior gate control, but it still poses a challenge for consistent device operation in large-scale integration.

GAA FETs stand out among emerging transistor architectures, including Forksheet FETs and Vertical Transport FETs, by offering a well-balanced compromise between performance enhancement, scalability potential, and manufacturing feasibility. Forksheet FETs, for example, provide similar benefits in terms of scalability but with potentially lower leakage due to their unique structure. However, GAA FETs currently have a more mature manufacturing process, making them a more immediate candidate for integration into advanced technology nodes. Vertical Transport FETs, on the other hand, offer advantages in terms of reduced footprint and potential for high drive currents. Still, they face significant challenges in terms of process integration and reliability, particularly in the control of short-channel effects. GAA FETs, with their superior gate control, provide a more straightforward path forward for continuing Moore's Law.

4. Conclusion

Gate-All-Around (GAA) FETs represent a pivotal advancement in semiconductor technology, addressing critical limitations of traditional FinFETs as device scaling pushes into the sub-5nm node range. For instance, GAA FETs have demonstrated up to 50% improvement in drive current and 30% reduction in power consumption compared to FinFETs at equivalent nodes. The all-around gate structure of GAA FETs provides superior electrostatic control, leading to higher drive currents, lower leakage currents, and improved subthreshold swing, making them ideal for high-performance, low-power applications. The ongoing development of GAA FETs, with projected implementations in 3nm and 2nm nodes, underscores their potential to extend Moore's Law and semiconductor scaling well into the next decade, potentially enabling computing advancements in areas such as artificial intelligence and quantum computing. However, several challenges remain, particularly in managing SCEs and ensuring the long-

term reliability of these devices at extremely small nodes. Future work in GAA FETs will likely focus on materials innovation to further enhance performance and reliability. This may include the exploration of high-mobility channel materials like Germanium or III-V compounds, as well as the development of advanced gate dielectrics to mitigate SCEs more effectively. Additionally, process innovations, such as strain engineering and 3D integration, will be critical in optimizing the performance of GAA FETs. In conclusion, while GAA FETs offer significant improvements over previous technologies, ongoing research is needed to fully address remaining challenges, particularly in mitigating short-channel effects at ultra-scaled nodes.

References

[1] Sreenivasulu V. B., Narendar V. Circuit analysis and optimization of GAA nanowire FET towards low power and high switching. Silicon, 2022, 14(16): 10401-10411.

[2] Das R. R., Rajalekshmi T. R., James A. FinFET to GAA MBCFET: A Review and Insights. IEEE Access, 2024, 50556-50577.

[3] Kim S., Kim J., Jang D., Ritzenthaler R., Parvais B., Mitard J., et al. Comparison of temperature dependent carrier transport in FinFET and gate-all-around nanowire FET. Applied Sciences, 2020, 10(8): 2979.

[4] Chen Z., Lin Y. M., Rooks M. J., Avouris P. Graphene nano-ribbon electronics. Physica E: Low-dimensional Systems and Nanostructures, 2007, 40(2): 228-232.

[5] Bhuwalka K. K., Sedlmaier S., Ludsteck A. K., Tolksdorf C., Schulze J., Eisele I. Vertical tunnel field-effect transistor. IEEE Transactions on Electron Devices, 2004, 51(2): 279-282.

[6] Bury E., Chasin A., Kaczer B., Vandemaele M., Tyaginov S., Franco J., et al. Evaluating forksheet FET reliability concerns by experimental comparison with co-integrated nanosheets. In Proceedings of the 2022 IEEE International Reliability Physics Symposium (IRPS), 5A-2.