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RISC-V Leads the Future: Evolution and Outlook of CPU Architecture

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Abstract:

This essay mainly talked the development of CPU and some instruction set architecture based on RISCV. CPU is known as the Central Processing Unit, the main appliment is RISCV, Also the ARM architecture is characterized by a focus on the balance between low power consumption and high performance. Then X86, its significant advantage is its complex instruction set and excellent performance, so it can handle complex computational tasks. We also explore the Pipeline technology, it is a widely used parallel processing technology today. The design principle is to divide complex, multilevel combinational logic circuits into multiple levels. Then, we find some experiment data to explore our conclusion. We find that each has its own advantages and is better suited to different scenarios. In terms of performance, x86 offers superior capabilities but consumes more power, making it ideal for high-performance computing and server applications. ARM, on the other hand, excels in power efficiency and finds its primary use in mobile devices and embedded systems. RISC-V, known for its flexibility, allows for a balance between performance and power consumption based on specific requirements, making it suitable for highly customizable applications, IoT devices, and emerging high-performance computing markets. The advantages of each architecture in different fields depend on the specific application environment and demands placed on them.

Keywords:RISC-V ArchitectureCPU Performance Evaluation Pipeline Technology

1. Introduction

Chip is the cornerstone of the entire electronic information industry, at present, the global semiconductor market size of 320 billion U.S. dollars, 54% of the chips are exported to China, but the market share of domestic chips accounted for only 10%. China's chip industry annual imports need to consume more than $200 billion in foreign exchange, more than oil and commodities, in the import of goods accounted for a considerable proportion[1]. The CPU as the heart of the chip, is the "core of the heart". And, the core position in the modern computer system is irreplaceable. It is not only the brain of the computer, responsible for the implementation of all instructions and data processing tasks, or connect and coordinate the work of the various components of the computer is the key hub, in the construction and design of computer systems, we must take into account the importance and role of the CPU.

CPU, as the core component of computer system, its development history, status quo and future trends reflect the continuous progress and innovation of computer technology. Academics, through the study of the development history of the CPU, to promote technological innovation, can reveal the internal law and power mechanism of technological progress, and provide theoretical support for future technological innovation. Its CPU technology involves a number of scientific fields such as computer science, electronic engineering, materials science, etc., which can promote the cross-fertilization and synergistic innovation among different disciplines. In industry, the development of CPU technology is an important force to promote the upgrading of computer industry and information technology industry. By actively adopting advanced CPU technology, it can promote the upgrading and transformation of the relevant industrial chain. In summary, the development of CPU has an extremely important role in both industry and academia.

2. Review of Literature

2.1 CPU Concept and Classification

CPU is known as the Central Processing Unit, that is, the central processing unit. It is an ultra-large-scale integrated circuit, which is the computing core (Core) and control core (Control Unit) of a computer. It integrates a large

number of transistors and other electronic components, used to execute the instructions in the computer program. It consists of three parts: the main control unit, the computing unit, and the storage unit, which are connected through the internal bus of the CPU.

An instruction set, as the name suggests, is a collection of instructions. The instruction set architecture is the main criterion for differentiating different CPUs. It is mainly categorized into Complex Instruction Set CISC and Reduced Instruction Set RISC. CISC not only contains instructions commonly used by the processor, but also includes many special instructions that are not commonly used, which is known as Complex Instruction Set because of its large number of instructions.RISC only contains instructions commonly used by the processor, and for the infrequently used operations, the same effect is achieved by executing a variety of commonly used instructions[2]. RISC is gradually becoming the mainstream instruction set design for mobile devices and embedded systems. RISC is gradually becoming the mainstream instruction set design for mobile devices and embedded systems. It incorporates techniques such as partially long instructions, chaotic execution, and multiple launches to improve the overall performance of the processor. The emergence of open-source instruction sets such as RISC-V has further contributed to the popularity and development of the RISC architecture.

2.2 Mainstream CPU Vendors and Development History

The history of the rivalry between AMD (Advanced Micro Devices) and Intel (Intel Corporation) is a semiconductor industry epic filled with technological innovations, market games, and shifting business strategies. The two companies have been both competitors and complementary players for decades, and together they have shaped the processor market as it exists today. The rivalry between Intel and AMD has a long history, spanning almost the entire evolution of personal computer processors. The two companies have competed fiercely in technology, markets, and products, and this competition has not only driven technological advances and innovations on both sides, but has also contributed to the development of the industry as a whole.

The two companies also have a cooperative relationship, which is mainly reflected in technical exchanges and resource sharing. For example, in technology, the two companies have had close cooperation, and even in some periods, AMD's CPU can be compatible with Intel motherboards, a CPU at the same time appear AMD and Intel Logo. In addition, industry experts also pointed out that Intel and AMD have formed a tacit understanding between the friendly game of relations, and even in some cases of reverse transportation of technology, to ensure that the two can rely on each other and coexist. To ensure that the two can coexist with each other. The existence of such a cooperative relationship, but also because if Intel a dominant, monopolizing the x86 CPU market, it is easy to be sanctioned by the antitrust authorities .

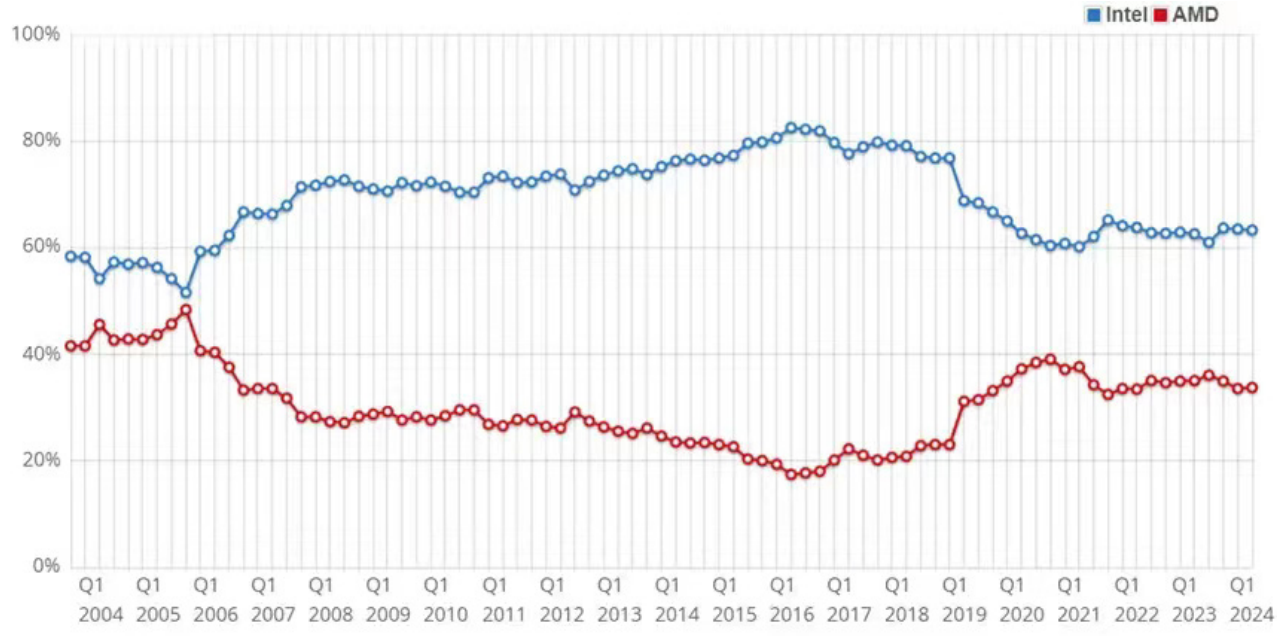

Fig. 1 AMD's and Intel's share of WB sales

AS shown in Fig.1,The two companies grew closer to each other in competition with each other.

2.3 Current Status of Domestic CPU Development

Chip is the cornerstone of the entire electronic information, the global semiconductor market up to 320 billion yuan, but the proportion of domestic chip share only reached ten percent. Central processing unit (Cpu) as the heart of the chip, but the proportion of domestic industry is relatively weak.

At present, China is in a critical period of vigorously developing the chip design industry, the realization of the great rejuvenation of the Chinese nation requires the majority of scientific research and engineering workers tireless efforts and hard work. At present, the domestic CPU industry is in the ascendant, and traditional commercial processors such as X86, ARM and MIPS show a blossoming trend.

In this context, the open RISC-V architecture brings great strategic opportunities to the development of China's CPU chip industry, and it is hoped that the domestic autonomy of Cpu and the mainstreaming of architecture can be realized completely. Mips system of Longxin and Junzheng, x86 system of the North Mass aspiration, Zhaoxin and Haikuang, power system in the Sheng Hongxin, alpha system of Shenwei and arm system of Fetion, Huawei Haisi, etc. These are the domestic independent research and development of cpu, and the development of the Chinese CPU industry has brought great strategic opportunities. These are domestic independent research and development of cpu company developed the chip subject, detailed understanding of which, you can find out exactly what causes the domestic commercial cpu has not yet succeeded, still with other development countries have a big gap.

Domestic CPUs are facing serious challenges in the international market. In recent years, with the continuous progress of technology and the enhancement of its own innovation ability, domestic CPU has gradually gained recognition in the international market. However, the competition in the CPU industry is extremely fierce, with Intel, AMD and other giant companies having strong technical support and market share. If domestic CPUs want to stand out in the international market, they need to continuously improve their technical strength and market share, and break through the technical and ecological barriers.

3. Basis of Methodological-technical Modeling

3.1 Instruction Set Architecture

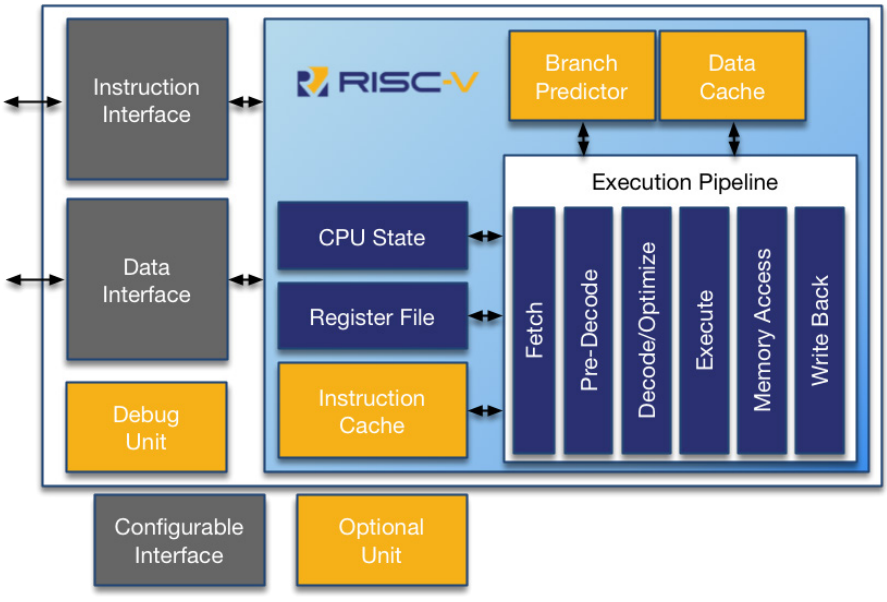

Fig. 2 Instruction Set Architecture[3]

AS shown in Fig.2, the RV12 implements the Harvard architecture for simultaneous instruction and data memory accesses. It has an optimized folded 6-stage pipeline. It optimizes the overlap between execution and memory accesses, thus reducing stalls and increasing efficiency. Opti onal features include branch prediction, instruction cache, data cache, debugging unit, and optional multiplier or divider unit. Parameterized and configurable features include instruction and data interfaces, branch prediction unit configuration, cache size, correlation, substitution algorithms, and multiplier delays. They provide users with trade-offs between performance, power consumption and

area to optimize the core of the application.

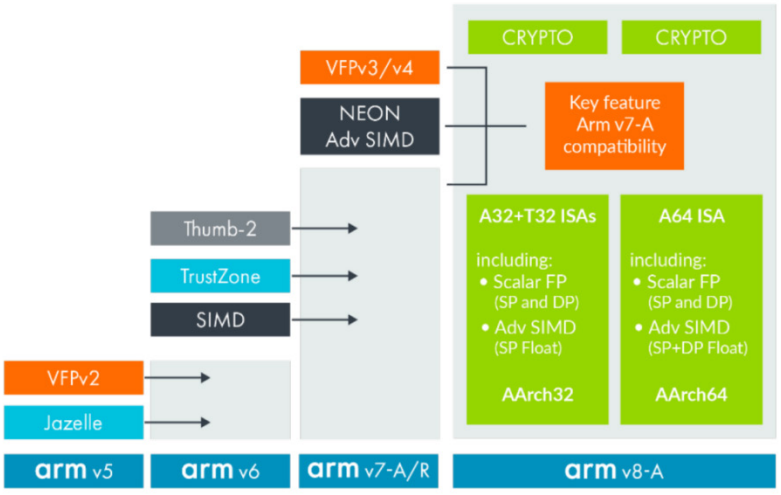

Fig. 3 Development of the Arm Architecture[4]

The ARM architecture has been developed over time, with each release building on previous. The Fig 3 shows the development of ARM from version five to version eight, it added a new feature each time in the process. We typically see this architecture referred to as Armv8-A, which is the eighth version of this architecture. The Armv8-A is a major milestone for Arm. Prior to the Armv7-A/R, the Arm architecture was a 32-bit architecture. Armv8-A is a 64-bit architecture, although it still supports 32-bit execution, providing backward compatibility for legacy software (e.g., v7, v6, and v5).

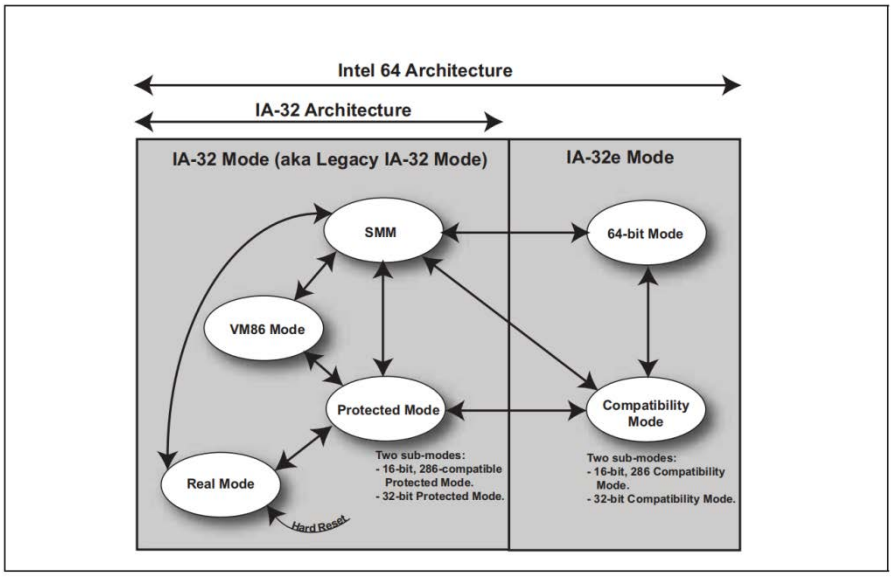

Fig . 4 Execution Mode

Intel 64 architecture processors can run in either IA-32 mode or IA-32e (IA-32 Extended) mode. The IA-32 architecture processor consists of the Real mode, System Management Mode (SMM), Protected Mode, VM86 Mode submode. The IA-32 Extended Mode consists of two submodes: 64-bit mode, and compatibility mode. The implementation has some advantages when executing the logic processor in IA-32e mode. For example, backward compatibility with the 1A-32 code environment; extending the size of the virtual memory address space from 4GB to 16EB (EB = exabytes); extends the size of the physical memory address space to 4PB(PB = petabytes); larger number of data registers allows for quick access/operation on a larger number of data variables, etc.

The three instruction sets have their own advantages in different scenarios. In terms of performance, x86 has more performance, but its power consumption is higher. Therefore, it is mainly used in high-performance computing and servers.ARM is better in terms of power efficiency and is mainly used in mobile devices and embedded systems. RISC-V, because of its more flexible nature, is free to balance its performance and power consumption according to its needs.It is mainly used in areas with high customization needs, IoT devices and high performance computing in emerging markets.All three have their own advantages in different areas, depending on the environment and the requirements of the application.

3.2 Pipeline Technology

Pipeline technology is a widely used parallel processing technology today. The design principle is to divide complex, multilevel combinational logic circuits into multiple levels. It divides an instruction into multiple steps which are then executed separately by these circuit units. Thus multiple instructions can overlap when the program is executed.

In the practical application of assembly line technology, we can insert registers into more complex combinational logic circuits so that they are broken down into simpler chunks. In this way, the overall system frequency will be determined by the maximum delay value of the combinational logic, thus increasing efficiency. Therefore, the problem of reducing the maximum value of delay is also very critical in the process of system design.

To further increase the performance of the CPU, the designer used a 5-stage pipeline in the CPU. The five-stage assembly line is divided as shown in .[5] The instructions can be divided into five stages: finger fetch stage, decode stage, emulate store stage, execute stage, and write back stage.

4. Applications

4.1 RISC-V Applications

RISCV is extremely flexible due to its open and lean instruction set based architecture. It has a trend in the market now towards customized IoT devices and high performance computers for emerging markets. Its main applications are in customized devices and high-performance computers as well as automotive chips.

Representative products based on this architecture include the SiFIVE Essantial series of high-performance processors developed by SiFive and the Gentei 9 series of Gentei processors [6].Among them, as a company that establishes and develops open source ecosystems, Xuan Tie, a subsidiary of Ali, is committed to promoting cutting-edge research on the RISC-V architecture based on the RISC-V architecture. At the Xuan Tie RISC-V Eco-Conference on March 14, 2024, Dharma Institute announced the launch of the “Swordless Alliance”. It is exploring a new paradigm of RISC-V industry cooperation with Synopsys, CoreTech, Qingdao Haier Technology Co. For example, Synopsys has deeply integrated simulation, debugging and verification tools with Xuan Tie CPUs, providing faster RISC-V hardware simulation. It has already been prototyped to validate SoC systems, assisting chipmakers to increase productivity and significantly reduce mass production risk.

4.2 ARM Applications

The ARM architecture is characterized by a focus on the balance between low power consumption and high performance. Of ARM’s multiple families of processors, Cortex-A is used for high performance and Cortex-M focuses on low power and real-time. At the same time, ARM uses a licensing model that allows other companies to design and manufacture processors based on ARM’s architecture. The above features allow it to shine in mobile devices and are mainly used in mobile devices, embedded systems and servers.

Representative companies using the ARM architecture include Apple, Qualcomm, Huawei Hesse, and others. Its representative products include Apple iPhone series, Kirin chips developed by Huawei’s Hath Semiconductor, and Raspberry Pi series. In recent years, Kirin chips have also made significant progress in scenario applications in the automotive chip field. For example, Huawei has signed a cooperation agreement with BYD to integrate the Kirin 710A into the digital cockpit of BYD models. It will be applied in the direction of in-vehicle entertainment systems, communications, and location-based navigation. The signing of this agreement marks the landing of Huawei Kirin chips in the automotive sector.

4.3 X86 Applications

The x86 architecture was originally developed by intel. Its significant advantage is its complex instruction set and excellent performance, which allows it to handle complex computational tasks. At the same time, x86 has a long and mature development history, and all aspects of technology are more mature. As a result, the X86 architecture is widely used in the PC and server markets.

The main processor products of this architecture are Zongzhi-805, which is based on North America’s Volkswagen UniCore-I microprocessor architecture, and Intel’s Intel 8086. Among other things, the introduction of the Intel 8086 not only defined the basis of the x86 architecture, but also became the foundation of the personal computer

compatibles market. It has had a profound impact on the development of personal computing technology.

5. Experiment

5.1 Peformance Ealuation Method

Dhrystone was developed by Reinhold P. Weicker in 1984 as a synthetic computing benchmark program aimed at representing system (integer) programming. It was designed to measure and compare the performance of different computing systems by running a set of typical general computing tasks. Originally written in Ada, Dhrystone was later ported to other programming languages and focuses on integer arithmetic, string handling, pointer operations, and other common programming tasks. Dhrystone primarily measures the performance of a CPU by determining how many Dhrystone programs it can execute per second (DMIPS, Dhrystones per second). A Dhrystone program includes a large number of integer arithmetic, conditional branches, array operations, and pointer references, among other common computing tasks. The Dhrystone benchmark program concentrates on integer arithmetic and basic control flow operations, which are crucial for most general computing tasks. The Dhrystone benchmark program simulates the computational requirements of typical applications by executing a series of fixed operations, such as loops, conditional statements, array operations, and function calls. After the test is completed, the DMIPS score is calculated based on the number of Dhrystone programs executed per second. This score provides a performance benchmark for the CPU in handling general integer calculations.

CoreMark is a computational performance benchmark program designed for embedded systems. It is intended to evaluate the performance of processor cores and was developed by EEMBC (Embedded Microprocessor Benchmark Consortium) to represent common processing workloads found in actual applications. CoreMark measures the performance of processor cores by executing a series of typical algorithms and tasks, including integer and floating-point operations, control flow, and memory access.The benchmark measures CPU performance, typically in units of how many CoreMark programs can be executed per second (CoreMark score). A CoreMark program includes a variety of operations such as integer and floating-point operations, control flow, and memory access. When assessing CPU performance, CoreMark attempts to cover a broader range of computational workloads, including integer and floating-point calculations, memory access patterns, and control flow operations. This allows it to better reflect the processor's performance in diverse application scenarios.During testing, the benchmark program executes a series of common computational tasks found in real-world applications, such as loops, conditional branches, encryption algorithms, sorting algorithms, and more. These tasks are designed to represent typical workloads of embedded applications. The resulting CoreMark score is a comprehensive indicator that considers the processor's performance across different types of computational tasks. A higher CoreMark score typically indicates better performance of the processor in handling embedded applications.

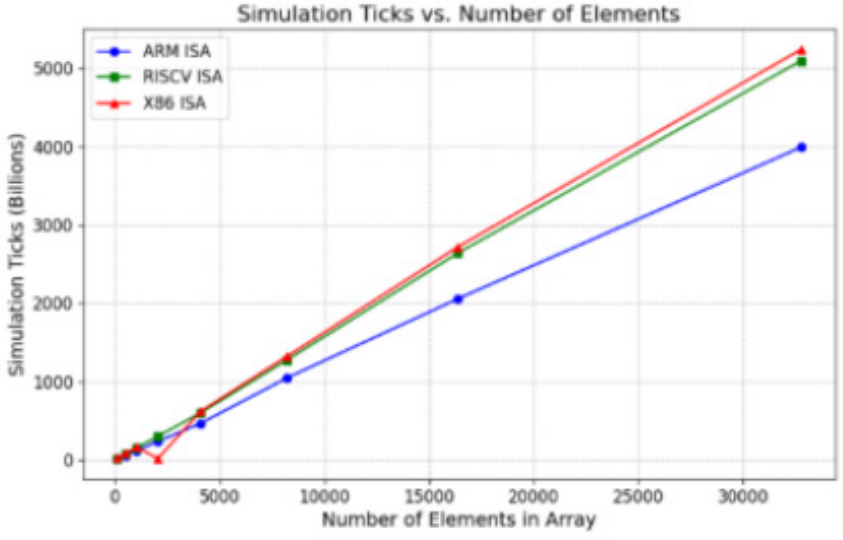

Fig. 5 Sim-Ticks Variation Across Different Number of Elements

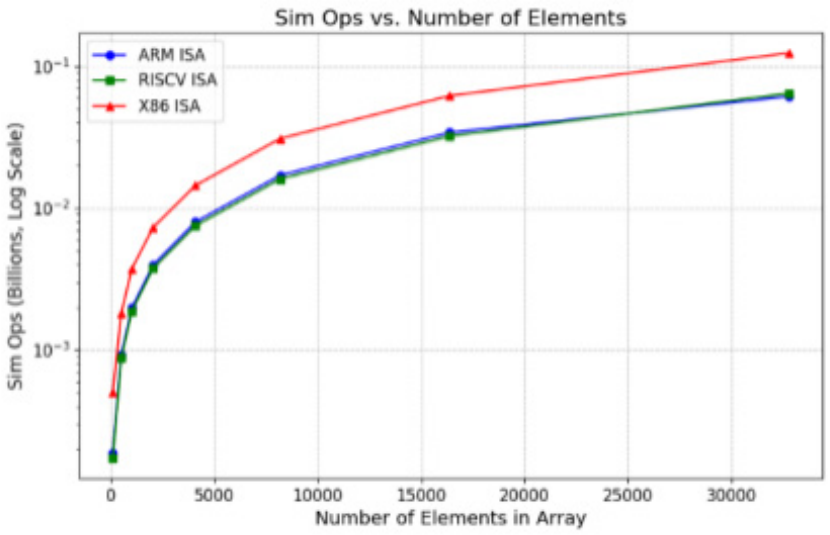

Fig. 6 Sim-Ops Variation with Different Number of Elements

Table 1. Three Scheme comparing

No of elements in array	ARM	RISCV	X86
100	0.1883	0.1733	0.5057
512	0.9288	0.8753	1.8168
1024	1.9839	1.8829	3.7387
2048	3.9561	3.7591	7.2972
4096	7.9682	7.5095	14.4239
8192	17.0019	16.0371	30.8756
16384	34.0607	32.1598	61.8142
32768	61.1621	64.31044	123.6229

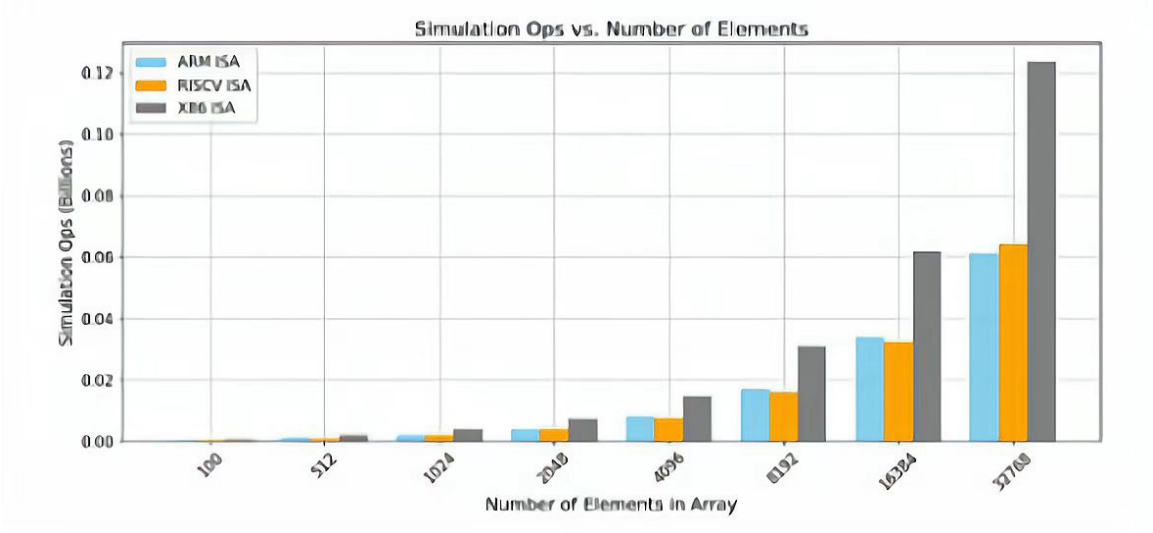

Fig. 7 Compare SimOps Histograms.

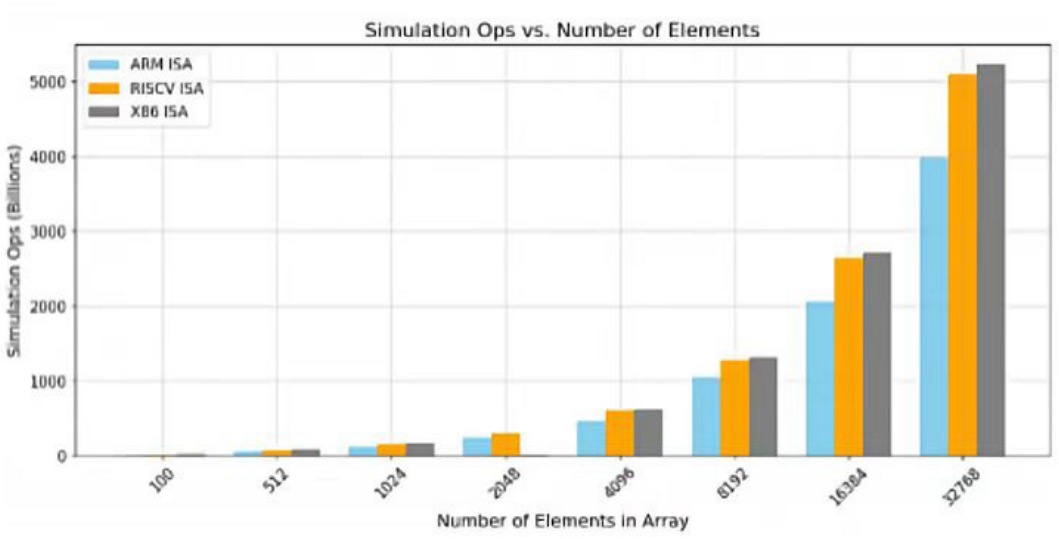

Fig. 8 Compare ARM RISCV X86 Histograms

5.2 Analysis of Experimental Results

First and foremost, as shown in figure 8, ARM stands out as the best performer among the three architectures. Compared to RISC-V and X86, it consistently demonstrates significantly higher speed and efficiency[7]. This superior performance can be attributed to ARM's architectural advantages and optimizations. When ARM leads, RISC-V closely follows. RISC-V exhibits commendable performance and efficiency, making it a powerful contender. While it may not match ARM's speed, it still notably surpasses X86. Conversely, X86 emerges as the poorest-performing ISA in this evaluation. The primary factor contributing to its slower performance is its reliance on Complex Instruction Set Computing (CISC) architecture. In contrast to the more streamlined and efficient ARM and RISC-V architectures, this inherently complex architecture leads to slower execution times. Overall, this evaluation demonstrates a clear hierarchy in terms of performance, with ARM in the lead, followed by RISC-V, and X86 as the slowest ISA. These findings underscore the importance of selecting the appropriate ISA for specific computing tasks to achieve optimal performance.In summary, a comprehensive comparative analysis was conducted on three prominent CPU architectures: X86, ARM, and RISC-V[8]. The focus of this study was to perform a specific application, radix sort, utilizing a simplified CPU timing model. Key performance parameters studied included cycles (simulated operations), SimTicks (simulated ticks), and CPI (cycles per instruction). With in-depth examination and analysis of these parameters, it becomes evident that the ARM architecture is a clear leader in both speed and efficiency. Following ARM, the RISC-V architecture demonstrates commendable performance, albeit slightly behind ARM.[9] In comparison, the X86 architecture lags behind both ARM and RISC-V in terms of performance. [9] This study emphasizes the importance of architecture selection when considering the execution of specific applications. The research results emphasize that for radix sorting, choosing the ARM architecture will result in the fastest execution, while RISC-V provides a competitive alternative.[10]

6. Conclusion

This article mainly studies the development and evolution of CPUs as well as the future prospects of CPUs. It mainly introduces three typical CPU architectures: RISC-V, X86, and ARM It traces their development history, their respective development processes, their current applications, and their future prospects. The article focuses on their performance and each has its own advantages. RISC-V is highly customizable and excels in the field of customization. X86 has better performance and is suitable for high-computing applications, but it consumes a high amount of power. ARM has relatively balanced power consumption but slightly weaker performance. Each of the three architectures demonstrates different roles and advantages in various demands.

The potential directions for future research in CPU architecture and technology include:Optimization and integration of multi-core processors: The advancement of Very Large Scale Integration (VLSI) technology enables the integration of more cores on a single chip. Future research will focus on optimizing the efficiency of multi-core processors, improving inter-core communication bandwidth, and reducing latency to achieve better performance scalability.

Authors Contribution

All the authors contributed equally and their names were listed in alphabetical order.

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